Claims

1. Electronic component containing:

- a multi-layer substrate (MS),

- at least one chip component (CB) having external contacts (AE), wherein the at least one chip component (CB) is disposed on the upper side of the multi-layer substrate (MS), characterized in that

at least one integrated impedance converter (IW) is disposed in the multi-layer substrate (MS), wherein the at least one chip component (CB) is electrically connected with the at least one integrated impedance converter (IW).

2. Component according to Claim 1,

in which the external contacts (AE) of the at least one chip component (CB) constitute SMD contacts.

3. Component according to Claim 1 or 2,

in which the multi-layer substrate (MS) comprises, in addition to the impedance converter, at least one additional integrated passive or active circuit element.

4. Component according to at least one of Claims 1 to 3,

in which the at least one chip component (CB) comprises at least one filter circuit.

5. Component according to at least one of Claims 1 to 4,

in which the at least one chip component (CB) comprises at least one resonator operating with surface acoustic waves.

6. Component according to at least one of Claims 1 to 5,

in which the at least one chip component (CB) comprises a resonator operating with bulk acoustic waves.

7. Component according to at least one of Claims 1 to 6,

in which the at least one chip component (CB) is a microwave ceramic filter.

8. Component according to at least one of Claims 1 to 7,

in which the at least one chip component (CB) is an LC chip filter.

9. Component according to at least one of Claims 1 to 8,

in which the at least one chip component (CB) is a stripline filter.

10. Component according to at least one of Claims 1 to 9,

in which at least one discrete passive or active circuit element (SE) is disposed on the upper side of the multi-layer substrate (MS).

11. Component according to at least one of Claims 1 to 10,

in which the at least one discrete circuit element (SE) disposed on the surface of the multi-layer substrate forms at least a part of a high-frequency circuit, an adjustment circuit, an impedance converter, an antenna circuit, a diode circuit, a high-pass filter, a low-pass filter, a band-pass filter, a band elimination filter, a power amplifier, a diplexer, a duplexer, a coupler, a directional coupler, a memory element, a balun or a mixer.

12. Component according to at least one of Claims 1 to 11,

in which the at least one discrete circuit element (SE) disposed on the surface of the multi-layer substrate forms at least a part of a high-frequency circuit, a duplexer or a diplexer, wherein said circuit element connects the at least one chip component (CB) with an antenna.

13. Component according to at least one of Claims 1 to 12,

in which the at least one circuit element integrated in the multi-layer substrate (MS) forms at least a part of a high-frequent circuit, an adjustment circuit, an antenna circuit, a diode circuit, a high-pass filter, a low-pass filter, a band-pass filter, a band elimination filter, a power amplifier, a diplexer, a duplexer, a coupler, a directional coupler, a memory element, a balun or a mixer.

14. Component according to Claim 13,

in which at least a part of an adjustment circuit integrated in the multi-layer substrate is formed as one or more strip conductors on the upper side of the multi-layer substrate for later fine-tuning.

15. Component according to at least one of Claims 1 to 14,

in which the multi-layer substrate (MS) comprises a plurality of adjustment circuits.

16. Component according to at least one of Claims 1 to 15,

in which the multi-layer substrate (MS) contains ceramic layers.

17. Component according to at least one of Claims 1 to 16,

in which the multi-layer substrate (MS) contains layers of silicone or silicone oxide.

18. Component according to at least one of Claims 1 to 17,

in which the multi-layer substrate (MS) contains layers of an organic material, such as plastic or laminate.

19. Component according to at least one of Claims 1 to 18,

in which at least one input and/or at least one output of the at least one chip component (CB) is used to conduct an asymmetrical signal.

20. Component according to at least one of Claims 1 to 19,

in which the at least one input and/or the at least one output of the at least one chip component (CB) is used to conduct a symmetrical signal.

21. Component according to at least one of Claims 1 to 20,

in which the connections to ground of the at least one chip component (CB) are connected with an adjustment circuit at least partially integrated in the multi-layer substrate against the reference ground of the overall component, wherein said adjustment circuit comprises at least one element selected from among a coil, a capacitor or a line segment.

22. Component according to at least one of Claims 1 to 21,

in which both the at least one chip component (CB) and the at least one discrete circuit element (SE) disposed on the upper side of the multi-layer substrate (MS) constitute SMD elements (surface mounted design elements).

23. Component according to at least one of Claims 1 to 22,

in which the at least one chip component (CB) comprises a housing (GE) having external contacts (AE).

24. Component according to at least one of Claims 1 to 23,

in which the at least one chip component (CB) is connected with the multi-layer substrate (MS) by means of wire bonding.

25. Component according to at least one of Claims 1 to 23,

in which the at least one chip component (CB) is connected with the multi-layer substrate (MS) by means of flip-chip technology.

26. Method for the production of the component according to at least one of Claims 23 to 25,

comprising the following steps:

- installation of a chip into a housing (GE),

- mounting of the housing onto a multi-layer substrate (MS).

27. Method according to Claim 26,

wherein the at least one discrete circuit element (SE) is mounted on the upper side of the multi-layer substrate (MS).

28. Method according to Claim 27,

wherein the at least one chip component (CB) and the at least one circuit element (SE) are attached to the upper side of the multi-layer substrate (MS) in the same fashion.

29. Method according to at least one of Claims 26 to 28,

wherein the at least one chip component (CB) disposed on the upper side of the multi-layer substrate and/or the at least one circuit element (SE) is mechanically stabilized with a casting compound.